In the Specification:

Please amend paragraph [0036] on page 9 as follows:

[0036] In the first preferred embodiment, a strained channel PMOS transistor 202 is coupled to an NMOS transistor 201 to form an inverter, as shown in Figure 2a. A first stressor 222 occupies a region proximate the sides of the PMOS channel 208 and comprises a non-negligible portion of the PMOS source 217 and PMOS drain 211 regions. Lattice-mismatch zones 223 define the junction of the first and second semiconductor materials [[206]] 226 and 222 in the PMOS transistor 202. It is noted that the figures are not necessarily drawn to scale. In fact, in the preferred embodiment, the stressor has a thickness of about a few hundred angstroms, while the source and drain region may have a depth of up to a thousand angstroms or more. Therefore, the stressor usually forms a small portion of the source/drain regions.